# Contents

**University de Piura (UDEP)**
Sillabus 2022-I

## 1. COURSE

CS221. Computer Systems Architecture (Mandatory)

## 2. GENERAL INFORMATION

| | | |
|---|---|---|
| **2.1 Credits** | : | 3 |
| **2.2 Theory Hours** | : | 2 (Weekly) |
| **2.3 Practice Hours** | : | 2 (Weekly) |
| **2.4 Duration of the period** | : | 16 weeks |
| **2.5 Type of course** | : | Mandatory |
| **2.6 Modality** | : | Face to face |
| **2.7 Prerrequisites** | : | CS1D2. Discrete Structures II. ($2^{nd}$ Sem) |

## 3. PROFESSORS

Meetings after coordination with the professor

## 4. INTRODUCTION TO THE COURSE

A computer scientist must have a solid knowledge of the organization and design principles of diverse computer systems, by understanding the limitations of modern systems they could propose next-gen paradigms. This course teaches the basics and principles of Computer Architecture. This class addreses digital logic design, basics of Computer Architecture and processor design (Instruction Set architecture, microarchitecture, out-of-order execution, branch prediction), execution paradigms (superscalar, dataflow, VLIW, SIMD, GPUs, systolic, multithreading) and memory system organization.

## 5. GOALS

- Provide a first approach in Computer Architecture.
- Study the design and evolution of computer architectures, which lead to modern approaches and implementations in computing systems.
- Provide fine-grained details of computer hardware, and its relation with software execution.
- Implement a simple microprocessor using Verilog language.

## 6. COMPETENCES

Nooutcomes

Nospecificoutcomes

## 7. TOPICS

| **Unit 1: Digital logic and digital systems (18)** | |
|---|---|
| **Competences Expected: b** | |
| **Topics** | **Learning Outcomes** |
| • Overview and history of computer architecture<br>• Combinational and sequential logic/Field programmable gate arrays as a fundamental combinational + sequential logic building block<br>• Abstraction models<br>• Computer-aided design tools that process hardware and architectural representations<br>• Register transfer notation/Hardware Description Language (Verilog/VHDL)<br>• Physical constraints (gate delays, fan-in, fan-out, energy/power) | • Describe the progression of technology devices from vacuum tubes to VLSI, from mainframe computer architectures to the organization of warehouse-scale computers [Familiarity]<br>• Comprehend the trend of modern computer architectures towards multi-core and that parallelism is inherent in all hardware systems [Usage]<br>• Explain the implications of the "power wall" in terms of further processor performance improvements and the drive towards harnessing parallelism [Usage]<br>• Articulate that there are many equivalent representations of computer functionality, including logical expressions and gates, and be able to use mathematical expressions to describe the functions of simple combinational and sequential circuits [Familiarity]<br>• Design the basic building blocks of a computer: arithmetic-logic unit (gate-level), registers (gate-level), central processing unit (register transfer-level), memory (register transfer-level) [Usage]<br>• Use CAD tools for capture, synthesis, and simulation to evaluate simple building blocks (eg, arithmetic-logic unit, registers, movement between registers) of a simple computer design [Familiarity]<br>• Evaluate the functional and timing diagram behavior of a simple processor implemented at the logic circuit level [Assessment] |
| **Readings :** [HH12], [PP05], [PH04], [JAs07], [HP06], [Par05], [Sta10], [PCh06] | |

| **Unit 2: Machine level representation of data (8)** | |
|---|---|
| **Competences Expected: g** | |
| **Topics** | **Learning Outcomes** |
| • Bits, bytes, and words<br>• Numeric data representation and number bases<br>• Fixed- and floating-point systems<br>• Signed and twos-complement representations<br>• Representation of non-numeric data (character codes, graphical data)<br>• Representation of registers and arrays | • Explain why everything is data, including instructions, in computers [Assessment]<br>• Explain the reasons for using alternative formats to represent numerical data [Familiarity]<br>• Describe how negative integers are stored in sign-magnitude and twos-complement representations [Usage]<br>• Explain how fixed-length number representations affect accuracy and precision [Usage]<br>• Describe the internal representation of non-numeric data, such as characters, strings, records, and arrays [Usage]<br>• Convert numerical data from one format to another [Usage] |
| **Readings :** [HH12], [PP05], [PH04], [JAs07], [HP06], [Par05], [Sta10], [PCh06] | |

| **Unit 3: Assembly level machine organization (8)** | |
|---|---|
| **Competences Expected: b,g** | |
| **Topics** | **Learning Outcomes** |
| • Basic organization of the von Neumann machine<br>• Control unit; instruction fetch, decode, and execution<br>• Instruction sets and types (data manipulation, control, I/O)<br>• Assembly/machine language programming<br>• Instruction formats<br>• Addressing modes<br>• Subroutine call and return mechanisms<br>• I/O and interrupts<br>• Heap vs. Static vs. Stack vs. Code segments | • Explain the organization of the classical von Neumann machine and its major functional units [Familiarity]<br>• Describe how an instruction is executed in a classical von Neumann machine, with extensions for threads, multiprocessor synchronization, and SIMD execution [Familiarity]<br>• Describe instruction level parallelism and hazards, and how they are managed in typical processor pipelines [Familiarity]<br>• Summarize how instructions are represented at both the machine level and in the context of a symbolic assembler [Familiarity]<br>• Demonstrate how to map between high-level language patterns into assembly/machine language notations [Usage]<br>• Explain different instruction formats, such as addresses per instruction and variable length vs fixed length formats [Usage]<br>• Explain how subroutine calls are handled at the assembly level [Usage]<br>• Explain the basic concepts of interrupts and I/O operations [Familiarity]<br>• Write simple assembly language program segments [Usage]<br>• Show how fundamental high-level programming constructs are implemented at the machine-language level [Usage] |
| **Readings :** [HH12], [PP05], [PH04], [JAs07], [HP06], [Par05], [Sta10], [PCh06] | |

| **Unit 4: Functional organization (8)** | |
|---|---|
| **Competences Expected: b,g** | |
| **Topics** | **Learning Outcomes** |
| • Implementation of simple datapaths, including instruction pipelining, hazard detection and resolution<br>• Control unit: microprogrammed<br>• Instruction pipelining<br>• Introduction to instruction-level parallelism (ILP) | • Compare alternative implementation of datapaths [Assessment]<br>• Discuss the concept of control points and the generation of control signals using hardwired or microprogrammed implementations [Familiarity]<br>• Explain basic instruction level parallelism using pipelining and the major hazards that may occur [Usage]<br>• Design and implement a complete processor, including datapath and control [Usage]<br>• Determine, for a given processor and memory system implementation, the average cycles per instruction [Assessment] |
| **Readings :** [HH12], [PP05], [PH04], [JAs07], [HP06], [Par05], [Sta10], [PCh06] | |

| **Unit 5: Memory system organization and architecture (8)** | |
|---|---|
| **Competences Expected: b,g** | |
| **Topics** | **Learning Outcomes** |
| • Storage systems and their technology<br>• Memory hierarchy: importance of temporal and spatial locality<br>• Main memory organization and operations<br>• Latency, cycle time, bandwidth, and interleaving<br>• Cache memories (address mapping, block size, replacement and store policy)<br>• Multiprocessor cache consistency/Using the memory system for inter-core synchronization/atomic memory operations<br>• Virtual memory (page table, TLB)<br>• Fault handling and reliability<br>• Error coding, data compression, and data integrity | • Identify the main types of memory technology (eg, SRAM, DRAM, Flash, magnetic disk) and their relative cost and performance [Familiarity]<br>• Explain the effect of memory latency on running time [Familiarity]<br>• Describe how the use of memory hierarchy (cache, virtual memory) is used to reduce the effective memory latency [Usage]<br>• Describe the principles of memory management [Usage]<br>• Explain the workings of a system with virtual memory management [Usage]<br>• Compute Average Memory Access Time under a variety of cache and memory configurations and mixes of instruction and data references [Assessment] |
| **Readings :** [HH12], [PP05], [PH04], [JAs07], [HP06], [Par05], [Sta10], [PCh06] | |

| **Unit 6: Interfacing and communication (8)** | |
|---|---|
| **Competences Expected: b,g,i** | |
| **Topics** | **Learning Outcomes** |
| • I/O fundamentals: handshaking, buffering, programmed I/O, interrupt-driven I/O<br>• Interrupt structures: vectored and prioritized, interrupt acknowledgment<br>• External storage, physical organization, and drives<br>• Buses: bus protocols, arbitration, direct-memory access (DMA)<br>• Introduction to networks: communications networks as another layer of remote access<br>• Multimedia support<br>• RAID architectures | • Explain how interrupts are used to implement I/O control and data transfers [Familiarity]<br>• Identify various types of buses in a computer system [Familiarity]<br>• Describe data access from a magnetic disk drive [Usage]<br>• Compare common network organizations, such as ethernet/bus, ring, switched vs routed [Assessment]<br>• Identify the cross-layer interfaces needed for multimedia access and presentation, from image fetch from remote storage, through transport over a communications network, to staging into local memory, and final presentation to a graphical display [Familiarity]<br>• Describe the advantages and limitations of RAID architectures [Familiarity] |
| **Readings :** [HH12], [PP05], [PH04], [JAs07], [HP06], [Par05], [Sta10], [PCh06] | |

| **Unit 7: Multiprocessing and alternative architectures (8)** | |
|---|---|
| **Competences Expected: i** | |
| **Topics** | **Learning Outcomes** |
| • Power Law<br>• Example SIMD and MIMD instruction sets and architectures<br>• Interconnection networks (hypercube, shuffle-exchange, mesh, crossbar)<br>• Shared multiprocessor memory systems and memory consistency<br>• Multiprocessor cache coherence | • Discuss the concept of parallel processing beyond the classical von Neumann model [Assessment]<br>• Describe alternative parallel architectures such as SIMD and MIMD [Familiarity]<br>• Explain the concept of interconnection networks and characterize different approaches [Usage]<br>• Discuss the special concerns that multiprocessing systems present with respect to memory management and describe how these are addressed [Familiarity]<br>• Describe the differences between memory backplane, processor memory interconnect, and remote memory via networks, their implications for access latency and impact on program performance [Assessment] |
| **Readings :** [HH12], [PP05], [PH04], [JAs07], [HP06], [Par05], [Sta10], [PCh06] | |

| Unit 8: Performance enhancements (8) | |
|---|---|
| **Competences Expected: g,i** | |
| **Topics** | **Learning Outcomes** |
| • Superscalar architecture<br>• Branch prediction, Speculative execution, Out-of-order execution<br>• Prefetching<br>• Vector processors and GPUs<br>• Hardware support for multithreading<br>• Scalability<br>• Alternative architectures, such as VLIW/EPIC, and Accelerators and other kinds of Special-Purpose Processors | • Describe superscalar architectures and their advantages [Familiarity]<br>• Explain the concept of branch prediction and its utility [Usage]<br>• Characterize the costs and benefits of prefetching [Assessment]<br>• Explain speculative execution and identify the conditions that justify it [Assessment]<br>• Discuss the performance advantages that multithreading offered in an architecture along with the factors that make it difficult to derive maximum benefits from this approach [Assessment]<br>• Describe the relevance of scalability to performance [Assessment] |
| **Readings :** [HH12], [PP05], [PH04], [JAs07], [HP06], [Par05], [Sta10], [PCh06] | |

## 8. WORKPLAN

### 8.1 Methodology

Individual and team participation is encouraged to present their ideas, motivating them with additional points in the different stages of the course evaluation.

### 8.2 Theory Sessions

The theory sessions are held in master classes with activities including active learning and roleplay to allow students to internalize the concepts.

### 8.3 Practical Sessions

The practical sessions are held in class where a series of exercises and/or practical concepts are developed through problem solving, problem solving, specific exercises and/or in application contexts.

## 9. PLANNING

| DATE | TIME | SESSION TYPE | PROFESSOR |
|---|---|---|---|
| See at EDU | See at EDU | See at EDU | See at EDU |

## 10. EVALUATION SYSTEM

********* EVALUATION MISSING ********

## 11. BASIC BIBLIOGRAPHY


[HH12] David Harris and Sarah Harris. *Digital Design and Computer Architecture*. 2nd. Morgan Kaufmann, 2012. ISBN: 978-0123944245.

[HP06] J. L. Hennessy and D. A. Patterson. *Computer Architecture: A Quantitative Approach*. 4th. San Mateo, CA: Morgan Kaufman, 2006.

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[Par05] Behrooz Parhami. *Computer Architecture: From Microprocessors to Supercomputers*. New York: Oxford Univ. Press, 2005. ISBN: ISBN 0-19-515455-X.

[PCh06] Pong P.Chu. *RTL Hardware Design Using VHDL*. 1st. Wiley-Interscience, 2006.

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[Sta10] William Stalings. *Computer Organization and Architecture: Designing for Performance*. 8th. Upper Saddle River, NJ: Prentice Hall, 2010.